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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
JACKSON, BLANE J	

ART UNIT	PAPER NUMBER
2618	

NOTIFICATION DATE	DELIVERY MODE
11/05/2007	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

Docketing@eschweilerlaw.com

Office Action Summary	Application No.	Applicant(s)	
	10/822,544	PFANN ET AL.	
	Examiner	Art Unit	
	Blane J. Jackson	2618	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 August 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

Applicant's arguments with respect to claims 1-24 have been considered but are moot in view of the new ground(s) of rejection. Secondary prior art Claxton and Auvray where introduced to teach a first and second frequency divider coupled between a first PLL and a respective mixer and ADC. With a further search of the prior art, Petersson was found that clearly teaches both frequency dividers applied in the same receiver in accordance with the claim language. Consequently, primary prior art Boos that teaches a known transceiver configuration, is reapplied in combination with Petersson in the Non-Final rejection to follow.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Boos (US 7,103,343) in view of Petersson et al. (US 2003/0171100).

As to claim 1, Boos teaches an integrated transceiver circuit (figure 2, a transceiver operating in the GSM and UMTS standard with high integration density, column 1, lines 15-43) comprising:

A reception path including a mixer unit for demodulating a received signal and also including an analog/digital converter unit connected downstream from the mixer unit (figures 1 and 2, column 4, lines 10-24), and

A first voltage controlled oscillator (figure 2, column 5, line 62 to column 6, line 2, VCO of PLL1 which is the local oscillator for the receive path).

Boos teaches a *first amplifier* connected between the first voltage controlled oscillator and the mixer unit, figure 2, amplifier (V) at the output of PLL1, and a frequency multiplier or divider may or may not be used connected between the *reference oscillator* and the analog/digital converter unit for obtaining a sampling frequency for use by the analog/digital converter unit, column 5, lines 31-40, but does not teach a second frequency divider connected between the first voltage controlled oscillator and the analog/digital converter unit or a first frequency divider connected between the first voltage controlled oscillator and the mixer unit.

Petersson teaches a radio receiver comprising an antenna (12), front end (14), a mixer (16) using a local oscillator signal to shift the received signal into a frequency range suitable for sampling by an analog to digital converter (22), figure 2, paragraph 0019. Petersson discloses a master oscillator or PLL for channelized control of the different received channels, coupled to a frequency changer (28) comprising a first divider (32) and a second divider (34) to generate the design selected local oscillator frequency to the mixer and the sampling clock frequency to the analog-to-digital converter (ADC), paragraphs 0020-0022.

Since Boos teaches a transceiver designed with respect to the reference frequency and the PLL circuits are configured for a low-power requirement, a small chip area and is cost effective, column 2, lines 9-21, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the frequency generating circuits of Boos with respect to the frequency changer of Petersson such that the relationship between the local oscillator frequency and the analog-to-digital sampling rate eliminates aliased signals in the desired receive band and the baseband anti-aliasing filter may be removed from the circuit.

As to claim 2, Boos teaches the integrated transceiver circuit of claim 1 further including a transmission path having a modulator for modulating a signal to be transmitted, a second voltage controlled oscillator as the master oscillator for the transmit path, figure 2, VCO of PLL2. Boos teaches a *second amplifier (V)* connected between the first voltage controlled oscillator and the mixer unit, figure 2, amplifier (V) at the output of PLL2, but does not teach a third frequency divider connected between the second voltage controlled oscillator and the mixer unit.

Since Petersson teaches a frequency changer comprising a first divider coupled between a master oscillator and the receive path mixer, figure 2, paragraph 0020, it would have been obvious to one of ordinary skill in the art at the time of the invention to mirror the frequency changer of Petersson to the transmit circuits of the dual VCO system of Boos to simplify design.

As to claim 3 with respect to claim 2, Boos teaches a frequency multiplier or divider may be used to derive the correct timing signal to the transmit and receive path ADC's, column 5, lines 32-40 but does not teach a fourth frequency divider connected between the second voltage controlled oscillator and the digital/analog converter.

Since Petersson teaches a frequency changer comprising a second divider coupled between a master oscillator and the receive path ADC, figure 2, paragraph 0020, it would have been obvious to one of ordinary skill in the art at the time of the invention to mirror the frequency changer of Petersson to the transmit circuits of the dual VCO system of Boos to simplify design.

As to claims 4 and 17 with respect to claims 3 and 16, Boos teaches the integrated transceiver circuit including a reference frequency input for receiving an external reference frequency and a first phase locked loop connected between the reference frequency input and the first voltage controlled oscillator (figures 1 or 2, reference frequency (RG) coupled to PLL1 which comprises a VCO that outputs to drive the receive path mixer unit).

As to claim 5, Boos teaches the integrated transceiver circuit of claim 4 including a second phase locked loop connected between the reference frequency input and the second voltage controlled oscillator (figures 1 or 2, column 4, lines 54-67, frequency reference (RG) coupled to PLL2 comprising a voltage controlled oscillator (VCO)).

As to claims 6, 8, 10 and 14 with respect to claims 5, 4, 3 and 2, Boos teaches the reception path includes a digital signal processing unit connected downstream from the analog/digital converter unit, the digital signal processing unit having an output which forms a digital output of the reception path (figure 1, digital signal processing is implied in digital demodulator (DM1) positioned after the ADC).

As to claims 7, 9, 11 and 15 with respect to claims 6, 8, 10 and 14, Boos teaches the reception path includes a digital/analog converter unit coupled to the output of the DSP unit, the digital/analog converter unit having an output which forms an analog output of the reception path (figure 1, column 1, lines 16-35, a DAC is implied for at least the audio portion of a UMTS or GSM standard mobile telephone).

As to claims 12 and 16 with respect to claims 3 and 2, Boos teaches the integrated transceiver circuit including a reference frequency input for receiving an external reference frequency, and a phase locked loop connected between the reference frequency input and the second voltage controlled oscillator (figures 1 and 2, column 4, lines 54-67, reference frequency (RG) coupled to PLL2).

As to claim 13, Boos teaches the integrated transceiver circuit of claim 3 wherein the transmission path includes a low-pass filter unit connected between the digital/analog converter unit and the modulator (figure 2, filter (TP) between the DAC (DA) and modulator (M2, M2')).

As to claim 18 with respect to claim 2, Boos teaches the integrated transceiver circuit including a reference frequency input for receiving an external reference frequency and a first phase locked loop connected between the reference frequency input and the first voltage controlled oscillator (figures 1 and 2, column 4, lines 22-47, reference frequency (RG) coupled to PLL1).

As to claim 19, Boos teaches the integrated circuit of claim 2 wherein the modulator is an IQ modulator (figure 2, column 6, lines 3-16).

As to claim 20 with respect to claim 1, Petersson of Boos modified teaches the analog/digital converter unit includes first and second analog/digital converters having respective sampling control inputs which are connect to an output of the second frequency divider (figure 2, second divider (34) coupled to ADC (22)).

As to claim 21, Boos teaches the integrated transceiver circuit of claim 1 wherein the reception path includes a low-pass filter unit connected between the mixer unit and the analog/digital converter unit (figure 2, filters (TP) in the receive path).

As to claim 22, Boos teaches the integrated transceiver circuit of claim 1 wherein the mixer unit is an IQ mixer (figure 2, column 5, lines 41-61).

As to claim 23 with respect to claim 1, Petersson of Boos modified teaches the first and second frequency dividers are integer dividers (figure 2, paragraph 0020, frequency divider (32) and (34) divides the output of the master oscillator by any positive integer).

Claim 24 is rejected under 35 U.S.C. 103(a) as being unpatentable over Petersson et al. (US 2003/0171100) in view of Boos.

As to claim 24, Petersson teaches a method for processing a signal comprising:

Obtaining a demodulation frequency for use by a mixer unit in a reception path of an integrated transceiver circuit with a first frequency divider connected between a first voltage controlled oscillator and the mixer circuit (figure 2, paragraph 0020, frequency changer (28) comprising first divider (32) coupled between a master oscillator (30) and mixer (16)),

Demodulating a received signal with the mixer unit and the obtained demodulation frequency (figure 2, mixer (16)),

Obtaining a sampling frequency for use by an analog to digital converter unit with a second frequency divider connected between the first voltage controlled oscillator and the analog to digital converter unit (paragraph 0020, frequency changer (28) includes a second frequency divider (34) to derive a sampling frequency from a master oscillator (30) to ADC (22)),

Performing a digitizing operation on the demodulated received signal with the analog to digital converter and the obtained sampling frequency (figure 2, digital processing (26)).

Petersson teaches obtaining a demodulation frequency for use by a mixer unit in a reception path of an integrated receiver circuit, figure 2, t but does not teach an integrated transceiver.

Boos teaches a method for processing a signal comprising a reception path of an integrated transceiver circuit for application in the GSM or UMTS standard mobile radio telephone, figures 1 and 2, column 1, lines 15-43.

It would have been obvious to one of ordinary skill in the art at the time of the invention to further recognize the receiver of Petersson as employed or application in the transceiver of Boos for application in mobile radiotelephones.

Conclusion

The prior art made of record and not relied upon but considered pertinent to applicant's disclosure includes Matero et al. (US 6,125,266), Yoshida et al. (US 2002/0039894), Tanaka et al. (Us 2004/0137853) and Dubash et al. (US 6,675,003).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Blane J. Jackson whose telephone number is (571) 272-7890. The examiner can normally be reached on Monday through Friday, 9:00 AM-6:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Edward Urban can be reached on (571) 272-7899. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.